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**CLAIMS:**

What is claimed is:

- 5 1. A method in a multi-processor data processing system  
for managing processors, the method comprising:  
responsive to detecting a failed processor in a set  
of processors on a multi-chip module, identifying a spare  
processor on the multi-chip module; and  
10 assigning the spare processor to replace failed  
processor.
2. The method of claim 1, wherein the spare processor  
on the multi-chip module is marked for use as a spare.  
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3. The method of claim 1 further comprising:  
selecting another spare processor on a different  
multi-chip module if the spare processor is absent.
- 20 4. The method of claim 1, wherein the spare processor  
is marked by an open firmware.
5. A method in a data processing system for managing  
processors, the method comprising:  
25 monitoring for a failed processor in the processors;  
and

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responsive to detecting a failed processor,  
identifying a spare processor from a set of spare  
processors, wherein the set of spare processors are  
located on different modules and wherein the spare  
5 processor is identified as minimizing degradation in  
processing performance.

6. The method of claim 5, wherein the spare processor  
is selected from a module containing the failed  
10 processor.

7. The method of claim 6, wherein the spare processor  
is selected from a die containing the failed processor.

15 8. A multi-processor data processing system for  
managing processors, the data processing system  
comprising:

detecting means for detecting a failed processor in  
a set of processors on a multi-chip module, identifying a  
20 spare processor on the multi-chip module; and

assigning means for assigning the spare processor to  
replace failed processor.

9. The multi-processor data processing system of claim  
25 8, marking means for marking the spare processor on the  
multi-chip module for use as a spare.

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10. The multi-processor data processing system of claim 8 further comprising:

5 selecting means for selecting another spare processor on a different multi-chip module if the spare processor is absent.

11. The multi-processor data processing system of claim 8, marking means for marking the spare processor by an open firmware.

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12. A multi-processor data processing system in a data processing system for managing processors, the data processing system comprising:

15 monitoring means for monitoring for a failed processor in the processors; and

20 detecting means for detecting a failed processor, identifying a spare processor from a set of spare processors, wherein the set of spare processors are located on different modules and wherein the spare processor is identified as minimizing degradation in processing performance.

13. The multi-processor data processing system of claim 12, selecting means for selecting the spare processor 25 from a module containing the failed processor.

14. The multi-processor data processing system of claim 13, selecting means for selecting the spare processor from a die containing the failed processor.

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15. A computer program product in a computer readable medium for managing processors, the computer program product comprising:

5 first instructions responsive to detecting a failed processor in a set of processors on a multi-chip module, identifying a spare processor on the multi-chip module; and

second instructions assigning the spare processor to replace failed processor.

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16. The computer program product of claim 15, wherein the spare processor on the multi-chip module is marked for use as a spare.

15 17. The computer program product of claim 15 further comprising:

third instructions for selecting another spare processor on a different multi-chip module if the spare processor is absent.

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18. The computer program product of claim 15, wherein the spare processor is marked by an open firmware.

19. A computer program product in a computer readable medium in a data processing system for managing  
25 processors, the computer program product comprising:

first instructions for monitoring for a failed processor in the processors; and

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second instructions responsive to detecting a failed processor, identifying a spare processor from a set of spare processors, wherein the set of spare processors are located on different modules and wherein the spare  
5 processor is identified as minimizing degradation in processing performance.

20. The computer program product of claim 19, wherein the spare processor is selected from a module containing  
10 the failed processor.

21. The computer program product of claim 20, wherein the spare processor is selected from a die containing the failed processor.